AMENDMENT(S) TO THE SPECIFICATION:

Kindly amend the abstract on page 32 as follows:

-- An apparatus, a carrier medium storing instructions to implement a method, and a method in a node of a wireless network able to receive packets that exactly or substantially conform to a wireless network standard according to which each packet includes a header having bits that have respective correct values in the case that the packet exactly conforms to the standard. The method includes receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received, checking one or more bits in the header to determine whether or not they have their respective correct values, and continuing to process the packet in the case that the checking indicates that the checked bits have their respective correct values. In one implementation, the header includes a first field modulated at a known rate that has one or more ~~unused bits~~ reserved bit locations, and a second field modulated at a data rate indicated in the first field. In such an implementation, the checking includes processing the first field and checking one or more bits in the first field to determine whether or not they have their respective correct values, and, if the checked bits of the first field have their respective correct values, checking the second field for integrity. --

Kindly amend paragraph [0004] on page 2 as follows:

-- **[0004]** Disclosed herein is an apparatus, a carrier medium storing instructions to implement a method, and a method in a node of a wireless network able to receive packets. The packets exactly or substantially conform to a wireless network standard according to which each packet ~~includes a header having unused bits~~ has a header including reserved bit locations containing bits set to a known value and ~~bits having only~~ specified bit locations with bits set according to legal/expected combinations in the case that the packet exactly conforms to the standard. One embodiment of the method includes receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received, checking one or more bits in the header to determine

whether or not they have their respective preset values in the case of ~~unused bits~~ reserved bit locations or legal/expected combinations, and continuing to process the packet in the case that the bits of the header pass the test, e.g., that the checked ~~unused bits~~ reserved bit locations have their respective preset values and/or the combinations are not illegal or unexpected. We refer to header bits that have their preset values if they are ~~unused bits~~ reserved bit locations or header bits that do not have an illegal or unexpected combination as header bits that have "correct" values. --

Kindly amend paragraph [0005] on page 2 as follows:

-- **[0005]** In one embodiment, the header includes a first field modulated at a known rate that has one or more ~~unused bits~~ reserved bit locations, and a second field modulated at a data rate indicated in the first field. In such an embodiment, the checking includes processing the first field and checking one or more bits in the first field to determine whether or not they have their respective correct values, and, if the checked ~~unused bits~~ reserved bit locations of the first field have their respective correct values, checking the second field for integrity. --

Kindly amend paragraph [0006] on page 2 as follows:

--**[0006]** In one embodiment, the packet optionally includes an indication of whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code formed from at least part of the first field. In such an embodiment, checking the second field for integrity includes checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code. If it is ascertained that such an error detecting code is included, the checking includes checking the included error correcting code. If it is ascertained that an error detecting code is not included, the checking includes checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective preset values. --

Kindly amend paragraph [0017] on page 4 as follows:

--[0017] Described herein are a method and apparatus that can detect relatively early whether or not there is a false SOP trigger in a receiving node of a WLAN. Communication in the WLAN is in the form of packets, and each packet has a header. According to which WLAN standard the node conforms, e.g., one of the IEEE 802.11 OFDM standards, some ~~bits~~ bit locations in the header of the packet are "~~unused~~ reserved." Typically, these ~~unused bits~~ reserved bit locations have known values, e.g., 0, for packets that exactly conform to the standard. Furthermore, some bits in the header have only certain combinations that are legal. We refer to header bits that have their preset values if they are ~~unused bits~~ reserved bit locations or header bits that do not have illegal or an unexpected combination as header bits that have "correct" values. One implementation of the invention includes the transmitter building packets that are exactly conforming. At the receiving node, once an SOP trigger is received, one embodiment of the method examines these bits of the header of a packet after receiving a start-of-packet trigger in the receiving node to ascertain whether or not the bits meet the requirements for the particular standard, and hence whether the packet is valid, or the result of a SOP false trigger. In yet another aspect of the invention, some of the bits in the header, in particular some of the ~~unused bits~~ reserved bit locations in the SERVICE field of a header ~~that conforms~~ conforming to one of the IEEE 802.11 OFDM standards, ~~standards that according to the standard~~ are used by a non-conforming transmitter—a transmitter that "substantially" but not exactly conforms to the standard—to add error detecting, e.g., CRC bits to better detect errors in the SIGNAL field. At the receiving node, there is a reduced likelihood of a false trigger being seen as a valid packet, e.g., an incorrect SIGNAL field having a correct set of CRC bits. --

Kindly amend paragraph [0025] on page 6 as follows:

--**[0025]** The modulated payload in turn starts with the Physical Layer Control Protocol (PCLP) header. FIG. 2A shows a PCLP header 200 that conforms exactly to the OFDM variants of the IEEE 802.11 standard. The PCLP header starts with a 3-byte SIGNAL field 203 that is modulated at a low data rate, in particular, SIGNAL is modulated at BPSK at rate 1/2 and provides information about the packet, including the data rate at which the rest of the packet in encoded. One embodiment uses ~~unused bits~~ reserved bit locations in the SIGNAL field to check for receive packet integrity. Another embodiment further checks the SIGNAL field to ensure that the combinations of bits are not illegal or unexpected. The SIGNAL field 203 is followed by a 2-byte SERVICE field 205 that is modulated at the payload data rate specified in SIGNAL. One embodiment uses ~~unused bits~~ reserved bit locations in the SERVICE FIELD to check for receive packet integrity. The remainder of the packet—the PLCP Service Data Unit (PSDU)—includes DATA at the payload data rate specified in the SIGNAL field 203. –

Kindly amend paragraph [0026] on page 7 as follows:

--**[0026]** FIG. 2B shows the individual bits of the 5-byte PCLP header. The SIGNAL field 203 includes RATE field of 4 bits denoted **Rate[0]** through **Rate[3]** that provide information on the data rate. The RATE information determines the coding rate and the modulation method used. The RATE field is followed by a reserved bit 213 that is always 0, and a 12-bit LENGTH field whose bits are denoted **Length[0]** through **Length[11]**. The LENGTH field is followed by a parity bit 215. This is followed by 6-tail bits 217 of the SIGNAL field denoted **Tail[0]** through **Tail[5]** that are ~~unused bits~~ reserved bit locations that should ~~be~~ contain 0. Note that the SIGNAL field includes legal combinations. Consider the RATE field. There are 4 bits, i.e., 16 combinations, but only 8 are expected for a fully conforming packet. The LENGTH field similarly has illegal combinations, e.g., values above 1600. –

Kindly amend paragraph [0027] on page 7 as follows:

--[0027] The three-byte SIGNAL field 203 is followed by the two-byte SERVICE field 205 that includes 7 random scrambler initialization bits denoted **Scram_Init[0]** through **Scram_Init[6]**, and nine SERVICE field bits denotes **Service[7]** through **Service[15]**. The latter are ~~unused bits~~ reserved bit locations that should all ~~be~~ contain value zero to conform exactly to the OFDM IEEE 802.11 standards. –

Kindly amend paragraph [0028] on page 7 as follows:

--[0028] A prior art receiver conforming to the OFDM variants of the IEEE 802.11 standard examines the parity bit 215 to ~~determine whether to~~ verify received packet integrity. One bit does not offer high likelihood that a correct SIGNAL field was received. In such a prior art receiver, the receiver may continue receiving data and passing such data to the MAC processor until the MAC processor determines that an error has occurred, e.g., because the frame check sequence (FCS) field at the end of a MAC frame—a 32-bit CRC—is incorrect. –

Kindly amend paragraph [0029] on pages 7–8 as follows:

--[0029] A receiver implementing one or more aspects of the invention includes a controller that checks the integrity of a received packet by checking not only whether the parity bit of the SIGNAL bit is correct, but also whether one or more other specific bits of the SIGNAL field in PLCP Header 200 in any received packet have their correct value, e.g., zero for ~~unused bits~~ reserved bit locations, and expected combinations for other bits. Thus, for such embodiments, a transmitter is assumed to transmit packets wherein **Tail[0]** through **Tail[5]** are 0 to conform exactly to the OFDM IEEE 802.11 standards. In another embodiment, the controller further checks the SERVICE field to determine whether or not other specific ~~unused bits~~ reserved bit locations of the SERVICE field 205 in PLCP Header 200 in any received packet have their required value. Thus, for such embodiments, a transmitter is assumed to

transmit packets wherein **Service[7]** through **Service[15]** are zero to conform exactly to the OFDM IEEE 802.11 standards. Yet another embodiment includes non-exactly conforming, but substantially conforming packets wherein parts of the PLCP header are protected by a set of error detecting bits, e.g., CRC bits, that are placed in some of the ~~unused~~ reserved SERVICE field ~~bits~~ bit locations. For one such embodiment, a transmitter is assumed to transmit packets that include an indication that a CRC is used, and wherein **Service[8]** through **Service[15]** include the CRC of some or all of the SIGNAL field. The indication used in one embodiment is that **Service[8]** through **Service[15]** being all 0 indicates that CRC is not being used. --

Kindly amend paragraph [0042] on page 11 as follows:

--**[0042]** One aspect of the invention is enabling rapid false start-of-packet detection by the transmit processor setting particular bits of the PLCP header that are ~~unused~~ reserved to 0 and the receive processor ascertaining whether indeed such ~~unused bits~~ reserved bit locations are zero. Another aspect of the invention is checking that only correct combinations exist for at least some of the bits of a received header. –

Kindly amend paragraph [0050] on page 12 as follows:

--**[0050]** Operation of an embodiment of the AGC controller uses a finite state machine (FSM) and is described in more detail in U.S. Patent Application Serial No. ~~10/xxx,xxx~~ 10/622,175 filed July 17, 2003 to inventors Adams, et al., titled ADAPTIVE AGC IN A WIRELESS NETWORK RECEIVER, Attorney/Agent Ref. No. CISCO-7343. Such U.S. Patent Application Serial No. ~~10/xxx,xxx~~ 10/622,175 is incorporated herein by reference. --

Kindly amend paragraph [0069] on page 17 as follows:

--**[0069]** In another alternate embodiment, all the processing to determine whether or not an SOP is a false SOP trigger is carried out by the MAC processor rather than the receive signal processor. FIG. 7 shows a flow chart

of such an embodiment. In 703, the MAC waits for indication that SIGNAL field data is available, e.g., that in PPDU mode, the modem is ready for the MAC to accept the seven initial bytes, or in PSDU mode, that the registers in register set 327 contain the SIGNAL part of the PLCP header. Once an indication is made to the MAC processor, in step 705, for PSDU mode, the MAC processor checks the SIGNAL field data in the respective registers of the register set 327 of the modem for integrity, and in PPDU mode, the MAC processor checks the SIGNAL field for integrity by checking for ~~unused bits~~ reserved bit locations having their preset values, and in one embodiment, also ensuring that RATE and/or SIGNAL do not have illegal combinations. If SIGNAL fails the test (707), the MAC processor treats the data as noise (709). If SIGNAL passes the test, and once the SERVICE field data is available to the MAC processor, in step 711, the MAC processor checks the SERVICE field for integrity, as described above. If the SERVICE field passes the test (713), the MAC processor continues to receive and process the PSDU data. --